translating, in response to first translation information, the first bit group from the first position to a different position in a comparand;

translating the second bit group from the second position to a second position of the comparand in response to second translation information

selecting the first translation information in a first cycle and the second translation information in a second cycle; and

comparing the comparand with data stored in a CAM array.

6. (Amended) The method of claim 1, further comprising concurrently translating the first and second bit groups into the comparand.

7. (Amended) The method of claim 1, further comprising sequentially translating the first and second bit groups into the comparand.

14. (Amended) An apparatus, comprising:

a content addressable memory (CAM) array to receive a comparand; and

a translation circuitry having at least one first input, at least one second input, and at least one output, wherein the first input is configured to receive an input data having a plurality of bit groups, wherein a first bit group has a first position in the input data relative to other bit groups, wherein the second input is configured to receive translation information indicative of translation of the first bit group from the first position to a different position in a comparand, the output coupled to the CAM array to transmit the comparand to the CAM array, and wherein the translation circuitry comprises:

a switch circuit;

a storage element to store the translation information; and

a decode circuitry coupled to the storage element to decode the translation information and to establish a connection in the switch circuit between the first position and the position in the comparand.

18. (Amended) The apparatus of claim 14, wherein the switch circuit comprises at least one demultiplexer.

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19. (Amended) The apparatus of claim 14, wherein the switch circuit comprises a cross-bar switch.

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21. (Amended) The apparatus of claim 14, further comprising an input bus coupled to the first input of the translation circuit and wherein the switch circuit comprises a plurality of multiplexers each coupled to the input bus.

29. (Amended) An apparatus, comprising:

a content addressable memory (CAM) array having a plurality of CAM blocks each configured to receive a comparand ; and

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a plurality of translation circuitry, each of the plurality of translation circuitry coupled to a corresponding one of the plurality of CAM blocks, each translation circuitry having at least one first input, at least one second input, and at least one output, wherein the first input is configured to receive an input data having a plurality of bit groups, wherein a first bit group has a first position in the input data relative to other bit groups, wherein the second input is configured to receive translation information indicative of translation of the first bit group from the first position to a different position in the comparand receive by a respective CAM block, the output coupled to transmit the comparand to the CAM block, wherein each of the plurality of translation circuitry is configured to translate the plurality of bit groups over multiple operation cycles.

43. (Amended) An apparatus comprising:

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a content addressable memory (CAM) array; and

means for translating, in response to translation information, a bit group from a position of an input data having a plurality of bit groups to a different position in a comparand, wherein the means for translating comprises:

means for storing the translation information; and

means for decoding the translation information.

45. (Amended) The apparatus of claim 44, wherein the translating comprises means for selecting the translation information from a plurality of translation information.

46. (Amended) An article comprising a machine readable medium that stores data representing an integrated circuit, comprising:

a content addressable memory (CAM) array to receive a comparand; and

a translation circuitry having at least one first input, at least one second input, and at least one output, wherein the first input is configured to receive an input data having a plurality of bit groups, wherein a first bit group has a first position in the input data relative to other bit groups, wherein the second input is configured to receive translation information indicative of translation of the first bit group from the first position to a different position in a comparand, the output coupled to the CAM array to transmit the comparand to the CAM array, wherein the translation circuitry further comprises:

a storage element to store the translation information; and

a decode circuitry coupled to the storage element to decode the translation information and to establish a switch circuit connection between the first position and the position in the comparand.

49. (Amended) A content addressable memory (CAM) device, comprising:

means for receiving an input data having a plurality of bit groups, wherein a first bit group has a first position in the input data relative to other bit groups, wherein the input data has a second bit group having a second position in the input data relative to other bit groups;

means for translating, in response to first translation information, the first bit group from the first position to a different position in a comparand;

means for comparing the comparand with data stored in a CAM array;

means for translating the second bit group from the second position to a second position of the comparand in response to second translation information; and

means for selecting the first translation information in a first cycle and the second translation information in a second cycle.

53. (Amended) The apparatus of claim 49, further comprising means for concurrently translating the first and second bit groups into the comparand.

54. (Amended) The apparatus of claim 49, further comprising means for sequentially translating the first and second bit groups into the comparand.

Please add the following new claims:

56. (New) An apparatus, comprising:

a content addressable memory (CAM) array to receive a comparand; and

a translation circuitry having at least one first input, at least one second input, and at least one output, wherein the first input is configured to receive an input data having a plurality of bit groups, wherein a first bit group has a first position in the input data relative to other bit groups, wherein the second input is configured to receive translation information indicative of translation of the first bit group from the first position to a different position in a comparand, the output coupled to the CAM array to transmit the comparand to the CAM array, wherein the translation circuitry comprises a switch circuit having at least one demultiplexer.

57. (New) The apparatus of claim 56, wherein the apparatus further comprises:

a plurality of storage elements, each of the plurality of storage elements to store a portion of the translation information;

selection circuitry coupled to the plurality of storage elements to select from among the plurality of storage elements; and

a decode circuitry coupled to the plurality of selection circuitry to decode the portion of the translation information and to establish a switch circuit connection between the first position and the position in the comparand.

58. (New) The apparatus of claim 57, wherein each of the plurality of storage elements to store a portion of the translation information for one cycles of a plurality of cycles, and the selection circuitry to select from among the plurality of storage elements based on a particular cycle of the plurality of cycles.

59. (New) The apparatus of claim 58, further comprising a comparand register coupled between the CAM array and the translation circuitry to store the comparand.

60. (New) The apparatus of claim 59, further comprising a processor coupled to the first input of the translation circuitry to transmit the input data.